

WEST Search History

DATE: Friday, October 07, 2005

<u>Hide?</u>	<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>
	<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>		
<input type="checkbox"/>	L57	L52 not L56	26
<input type="checkbox"/>	L56	L52 not L55	50
<input type="checkbox"/>	L55	L54 not L53	26
<input type="checkbox"/>	L54	vliw and L52	31
<input type="checkbox"/>	L53	L39 and L52	5
<input type="checkbox"/>	L52	global with broadcast\$3 with register\$1	76
<input type="checkbox"/>	L51	("6629232" "6401190" "6418527" "6317820" "5574939").PN.	5
<input type="checkbox"/>	L50	bops.as. and shared and local	6
<input type="checkbox"/>	L49	bops.as. and global and local	3
<input type="checkbox"/>	L48	bops.as. and (global same local)	0
<input type="checkbox"/>	L47	6366999.pn.	1
<input type="checkbox"/>	L46	L41 not L44	47
<input type="checkbox"/>	L45	L41 not L38L38	585
<input type="checkbox"/>	L44	L41 not L43	538
<input type="checkbox"/>	L43	L42 not sun.as.	47
<input type="checkbox"/>	L42	vliw and L41	76
<input type="checkbox"/>	L41	global register\$1	585
<input type="checkbox"/>	L40	global register\$1 and L39	11
<input type="checkbox"/>	L39	(712/24).ccls.	253
	<i>DB=USPT; PLUR=NO; OP=OR</i>		
<input type="checkbox"/>	L38	(synchroniz\$5 and vliw and 5574939.uref.)	10
	<i>DB=USPT; PLUR=NO; OP=ADJ</i>		
<input type="checkbox"/>	L37	synchroniz\$5 and L35	10
<input type="checkbox"/>	L36	synchriniz\$5 and L35	0
<input type="checkbox"/>	L35	vliw and L34	29
<input type="checkbox"/>	L34	5574939.uref.	56
	<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ</i>		
<input type="checkbox"/>	L33	5574939.uref.	0
<input type="checkbox"/>	L32	clustered vliw	2
<input type="checkbox"/>	L31	multiple vliw cores	0
<input type="checkbox"/>	L30	multiple vliw cores	0

<input type="checkbox"/>	L29	vliw and L28	12
<input type="checkbox"/>	L28	multiprocessor or multi-processor or (multiple processors)	13726
		<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L27	L12 with vliw	52
<input type="checkbox"/>	L26	clustered vliw	10
<input type="checkbox"/>	L25	variable issue width	10
<input type="checkbox"/>	L24	synchroniz\$5 same L23	4
<input type="checkbox"/>	L23	vliw processors	366
<input type="checkbox"/>	L22	multiple vliw cores	2
<input type="checkbox"/>	L21	multiple vliw processors	0
<input type="checkbox"/>	L20	multiple vliw pipelines	0
<input type="checkbox"/>	L19	vliw same L18	25
<input type="checkbox"/>	L18	multiple pipelines	475
<input type="checkbox"/>	L17	vliw and L16	5
<input type="checkbox"/>	L16	5459798.uref.	24
<input type="checkbox"/>	L15	vliw same L14	4
<input type="checkbox"/>	L14	L12 with chip	1282
<input type="checkbox"/>	L13	L12 adj chip	74
<input type="checkbox"/>	L12	multiprocessor or multi-processor or (multiple processors)	33673
<input type="checkbox"/>	L11	vliw and L10	6
<input type="checkbox"/>	L10	pipeline paths	26
<input type="checkbox"/>	L9	L7 same L8	12
<input type="checkbox"/>	L8	"two register files"	183
<input type="checkbox"/>	L7	"single register file"	165
<input type="checkbox"/>	L6	L3 not L5	156
<input type="checkbox"/>	L5	L3 not L2	190
<input type="checkbox"/>	L4	L2 and L3	156
<input type="checkbox"/>	L3	(global same broadcast\$3 same register\$1)	346
<input type="checkbox"/>	L2	(global same local same broadcast\$3 same register\$1)	156
<input type="checkbox"/>	L1	(global same local same broadcast\$3)	1149

END OF SEARCH HISTORY